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Class	Subclass
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ISSUE CLASSIFICATION

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PATENT NUMBER

U.S. UTILITY Patent Application

O.I.P.E.

PATENT DATE

SCANNED 15-4 Q.A. Ed

APPLICATION NO. 09/940749	CONT/PRIOR	CLASS 712 716	SUBCLASS 17	ART UNIT 2183 2825	EXAMINER Thompson
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APPLICANTS

James Lie

TITLE

Method and/or architecture for generating superset pinout for devices with combined programmable logic and high-speed serial channels

PTO-2040
12/99

ISSUING CLASSIFICATION

ISSUING CLASSIFICATION															
ORIGINAL				CROSS REFERENCE(S)											
CLASS		SUBCLASS		CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)										
INTERNATIONAL CLASSIFICATION															

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<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner) _____ (Date) _____ (Primary Examiner) _____ (Date) _____ (Legal Instruments Examiner) _____ (Date)			NOTICE OF ALLOWANCE MAILED	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____ _____ _____				ISSUE FEE Amount Due _____ Date Paid _____	
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